Power-Aware DVFS on IBM PowerPC 405LP: Front Bus Scaling

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OBJECTIVE:

Implementation of dynamic voltage and frequency scaling for the memory subsystem/front bus, and to study the power savings thus achieved on the IBM PowerPC 405LP board.

MOTIVATION:

Power management is an important design aspect of embedded systems design, especially for battery constrained devices. Various power optimization techniques have been proposed which offer power reduction while maintaining the safe operation of the system. Many processors support different power saving modes. Power saving modes like sleep and suspend involve lot of overhead for hard real-time systems. Recently many processors added support for Dynamic Power Management (DPM) techniques which allow power parameters such as voltage and frequency to be changed even while a program is in execution [1].

Dynamic Voltage Scaling (DVS) and Dynamic Frequency Scaling (DFS) are the most widely deployed DPM techniques. Dynamic power management techniques when applied only to scale the voltage and frequency of processor core can be of limited use [2]. Latest technological advances in processor design has lead to the development of low-power processor cores. Power optimization on the already low power consuming processor core might not provide significant power savings.

In embedded systems, internal/external bus and memory also consume significant power, sometimes even more than the processor itself [3]. So voltage and frequency scaling can be expected to provide significant power optimization when applied to the internal/external bus and memory subsystem. The aim of this project would be to integrate DVS/DFS to the front bus and memory subsystem and study the power optimizations that can be achieved on the IBM PowerPC 405LP board.

PROJECT OVERVIEW:

MontaVista Linux enhanced with EDF-based feedback scheduling, to realize DVS/DFS for the IBM PowerPC 405LP, is already available. The entire system consists of 2 components (i) a task/subtask scheduler, which dispatches the highest priority task and (ii) DVS scheduler, which assigns a particular voltage/frequency setting to the processor for that particular subtask [4]. This operating point is derived by a complex PID feedback algorithm. The system was shown to produce significant power savings on the PowerPC 405 LP board.

In order, to extend this DVS/DFS to the memory subsystem we need to figure out memory related control parameters which could be monitored by the feedback mechanism. In addition to the already existing feedback controller we would implement another controller for deriving operating points for the memory subsystem. This would be passed on to the DVS scheduler, which could then assign appropriate operating point to the memory subsystem for the subtask's execution.

PROPOSED APPROACH:

The following would be the guidelines for our project implementation,

1. Firstly, we would familiarize ourselves with the PowerPC 405LP board and development environment. This would require code browsing and reading PowerPC 405 LP user manual.

2. We would look at ways to obtain the voltage/current measurements from the acquisition board through the comedi drivers under Linux.
3. We would understand the DPM module of the MontaVista Linux RTOS and learn how to set/change frequency for the front side bus and the memory subsystem.
4. We would understand the implementation of the existing PID feedback controller which would be useful if were to implement another PID feedback controller specific to the memory subsystem.
5. We would then figure out the parameters that should be monitored and used by the memory subsystem's feedback controller. This would be necessary for creating operating points for the tasks.
6. Finally this controller will be integrated with the scheduler so that frequency scaling could be applied to the memory subsystem and front bus during the corresponding subtask invocation.
7. The current and voltage measurements after the implementation of FSB scaling would be documented for further study.

PROJECT WEBSITE:
http://www4.ncsu.edu/~sselvar/csc714/

REFERENCES:

[1] A survey of design techniques for system-level dynamic power management
Benini, L.; Bogliolo, A.; De Micheli, G. Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 8, Issue 3, Jun 2000 Page(s): 299 - 316

[2] www.research.ibm.com/arl/publications/papers/DPM_V1.1.pdf

[3] System level power-performance trade-offs in embedded systems using voltage and frequency scaling of off-chip buses and memory(2002). by Kiran Puttaswamy, Kyu-won Choi, Jun Cheol Park, Vincent J. Mooney Iii, Abhijit Chatterjee, Peeter Ellervee. In Proceedings of International Symposium on System Synthesis (ISSS'02)

[4] Exploiting Synchronous and Asynchronous DVS for Feedback EDF Scheduling on an Embedded Platform by Y. Zhu and F. Mueller in ACM Transactions on Embedded Computing Systems, Vol. 7, No. 1, Dec 2007, pages 1-26.

[5] "Feedback EDF Scheduling of Real-Time Tasks Exploiting Dynamic Voltage Scaling" by Y. Zhu and F. Mueller in Real-Time Systems Journal, Vol. 31, No. 1-3, Dec 2005, pages 33-63.

[6] Power reduction techniques for microprocessor systems ACM Computing Surveys (CSUR) Volume 37, Issue 3 (September 2005) Pages: 195 - 237

[7] PowerPC 405 User Manual