Developing Code for Cell - Mailboxes

Course Code: L3T2H1-55
Cell Ecosystem Solutions Enablement
Course Objectives – Things you will learn

- Cell communication mechanisms
  - mailboxes (this course) and DMA (another course)
- Mailbox queues for PPE and SPU
- Mailbox features and characteristics
- How to read and write mailboxes
- SPU outbound mailboxes and example
- SPU inbound mailbox and example
- PPE mailbox queue – PPE and SPU calls
- SPU mailbox queue – PPE and SPU calls
Course Agenda

- **Cell Communication Mechanisms**
- **Mailboxes**
  - How Mailboxes Were Sent
  - Mailbox Channels and their Associated MMIO Registers
- **Reading and Writing Mailboxes**
- **SPU Outbound Mailboxes**
  - Writing SPU Write Outbound Mailbox Data
  - Waiting to Write SPU Write Outbound Mailbox Data
  - How to Poll for or Block on an SPU Write Outbound Mailbox Available Event
  - How PPE Software can read from the SPU Write Outbound Mailbox of an SPE
  - Example shows how PPE software can read from the SPU Write Outbound Mailbox of an SPE
- **SPU Inbound Mailbox**
  - SPU Read Inbound Mailbox Channel
  - SPU Read Inbound Mailbox vs. SPU Write Outbound Mailboxes
  - How to write four 32-bit Messages to the PPU Read Inbound Mailbox of a Particular SPU from the PPE
- **PPE Mailbox Queue – PPE Calls, SPU Calls**
  - PPE Interrupting Mailbox Queue – PPE Calls
- **SPU Mailbox Queue – PPE Calls, SPU Calls**
- **Using mailboxes with macros defined in libspe.h and spu_mfcio.h**

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Overview Cell Communication Mechanisms

- **Mailboxes**
  - between PPE and SPEs

- **DMA**
  - between PPE and SPEs
  - between one SPE and another

- **Used for**
  - Synchronization
  - Error reporting
  - Communication
  - Monitor SPU status

**Some aspects of what is described are architecture and some aspects are implementation; e.g.:**

- queues are architecture
- queue sizes are implementation
Mailboxes

Each MFC provides three mailbox queues of 32 bit each:

1. **PPE ("SPU outbound") mailbox queue**
   - SPE writes, PPE reads
   - 1 deep
   - SPE stalls writing to full mailbox

2. **PPE ("SPU outbound") interrupt mailbox queue**
   - like PPE mailbox queue, but an interrupt is posted to the PPE when the mailbox is written

3. **SPU ("SPU inbound") mailbox queue**
   - PPE writes, SPE reads
   - 4 deep
   - can be overwritten

➢ Each mailbox entry is a fullword
Mailboxes Overview

PPU

MFC

PPE mbox
SPE out mbox

SPE mbox
in mbox

PPE intr mbox
SPE out intr mbox

SPU
Mailbox Architecture

- Find problem state address and offsets to memory mapped registers
- Write directly into memory

Channel Instructions:
- spu_writech(<channel>, <value>)
- spu_readch(<channel>)
- spu_readchcnt(<channel>)
How Mails Are Sent

- **SPE (outgoing)**
  - write the 32-bit message value to either its two outbound mailbox channels

- **SPE (incoming)**
  - reads a message in the inbound mailbox

- **PPE and other devices (incoming)**
  - read message in outbound mailbox by reading the MMIO register in the SPE’s MFC

- **PPE and other devices (outgoing)**
  - send by writing the associated MMIO register

- For interrupts associated with the SPU Write Outbound Interrupt Mailbox,
  - *no ordering of the interrupt and previously issued MFC commands*
# Mailbox Channels and their Associated MMIO Registers

<table>
<thead>
<tr>
<th>SPE Channel #</th>
<th>Name</th>
<th>Channel Interface</th>
<th>Max. Entries</th>
<th>Blocking</th>
<th>R/W</th>
<th>Width (bits)</th>
<th>Offset From Base</th>
<th>MMIO Register Interface</th>
<th>Mnemonic</th>
<th>Max. Entries</th>
<th>R/W</th>
<th>Width (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>SPU Write Outbound Mailbox</td>
<td>SPU_WrOutMbox</td>
<td>1</td>
<td>yes</td>
<td>W</td>
<td>32</td>
<td>X'04004'</td>
<td>SPU_Out_Mbox</td>
<td>1</td>
<td>R</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>SPU Read Inbound Mailbox</td>
<td>SPU_RdInMbox</td>
<td>4</td>
<td>yes</td>
<td>R</td>
<td>32</td>
<td>X'0400C'</td>
<td>SPU_In_Mbox</td>
<td>4</td>
<td>W</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>SPU Write Outbound Mailbox¹</td>
<td>SPU_WrOutInstrMbox</td>
<td>1</td>
<td>yes</td>
<td>W</td>
<td>32</td>
<td>X'04000'</td>
<td>SPU_Out_Intr_Mbox</td>
<td>1</td>
<td>R</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SPU Mailbox Status</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>X'04014'</td>
<td>SPU_Mbox_Status</td>
<td>1</td>
<td>R</td>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

1. Access to this MMIO register is available only to privileged PPE software.

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## Functions of Mailbox Channels (SPU)

<table>
<thead>
<tr>
<th>Channel Interface</th>
<th>SPU Read or Write</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPU_WrOutMbox</td>
<td>W</td>
<td>Writes message data to the outbound mailbox.</td>
</tr>
<tr>
<td>SPU_RdInMbox</td>
<td>R</td>
<td>Returns the next message data from the inbound mailbox</td>
</tr>
<tr>
<td>SPU_WrOutInstrMbox</td>
<td>W</td>
<td>Writes message data to the outbound interrupt mailbox.</td>
</tr>
</tbody>
</table>
## Functions of Mailbox MMIO Registers (PPU)

<table>
<thead>
<tr>
<th>MMIO Register</th>
<th>PPE Read or Write</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPU_Out_Mbox</td>
<td>R</td>
<td>Returns the message data from the corresponding SPU outbound mailbox.</td>
</tr>
<tr>
<td>SPU_In_Mbox</td>
<td>W</td>
<td>Writes message data to the SPU inbound mailbox.</td>
</tr>
<tr>
<td>SPU_Out_Intr_Mbox¹</td>
<td>R</td>
<td>Returns the message data from the corresponding SPU outbound interrupt mailbox.</td>
</tr>
<tr>
<td>SPU_MboxStat</td>
<td>R</td>
<td>Returns the number of available mailbox entries.</td>
</tr>
</tbody>
</table>

¹ Access to the SPU_Out_Intr_Mbox MMIO register is available only to privileged PPE software.
Reading and Writing Mailboxes
SPU Outbound Mailboxes
SPU Outbound Mailboxes

- **SPU Write Outbound Mailbox Channel**
  - The value **written** to the SPU Write Outbound Mailbox channel SPU_WrOutMbox is entered into the outbound mailbox in the MFC if the mailbox has capacity to accept the value.
  - If the mailbox can **accept** the value, the channel count for SPU_WrOutMbox is decremented by ‘1’.
  - If the outbound mailbox is **full**, the channel count will read as ‘0’.
  - If SPE software writes a value to SPU_WrOutMbox when the channel count is ‘0’, the SPU will **stall** on the write.
  - The SPU **remains stalled** until the PPE or other device reads a message from the outbound mailbox by reading the MMIO address of the mailbox.
  - When the mailbox is **read** through the MMIO address, the channel count is incremented by ‘1’.
SPU Outbound Mailboxes (Cont’d)

- **SPU Write Outbound Interrupt Mailbox Channel**
  - The value **written** to the SPU Write Outbound Interrupt Mailbox channel (SPU_WrOutIntrMbox) is entered into the outbound interrupt mailbox if the mailbox has capacity to accept the value.
  - If the mailbox can **accept** the message, the channel count for SPU_WrOutIntrMbox is decremented by ‘1’, and an **interrupt is raised** in the PPE or other device, depending on interrupt enabling and routing.
  - There is no ordering of the interrupt and previously issued MFC commands.
  - If the outbound interrupt mailbox is **full**, the channel count will read as ‘0’.
  - If SPE software writes a value to SPU_WrOutIntrMbox when the channel count is ‘0’, the SPU will **stall** on the write.
  - The SPU **remains stalled** until the PPE or other device reads a mailbox message from the outbound interrupt mailbox by reading the MMIO address of the mailbox.
  - When this is done, the channel count is **incremented** by ‘1’.
Writing SPU Write Outbound Mailbox Data

- SPE software can write to the SPU Write Outbound Mailbox channel to put a mailbox message in the SPU Write Outbound Mailbox.
- Sufficient space
  - Yes: immediate return
  - No: SPU will stall until the PPE reads from this mailbox
- How to write to the SPU Write Outbound Mailbox.
  ```c
  unsigned int mb_value;
  spu_writech(SPU_WrOutMbox, mb_value);
  ```
Waiting to Write SPU Write Outbound Mailbox Data

- To avoid SPU stall, SPU can use the read-channel-count instruction on the SPU Write Outbound Mailbox channel to determine if the queue is empty before writing to the channel.

- If the read-channel-count instruction returns ‘0’, the SPU Write Outbound Mailbox Queue is full.

- If the read channel-count instruction returns a non-zero value, the value indicates the number of free entries in the SPU Write Outbound Mailbox Queue.

- When the queue has free entries, the SPU can write to this channel without stalling the SPU.

- How to poll SPU Write Outbound Mailbox or SPU Write Outbound Interrupt Mailbox.

```c
/*
  * To write the value 1 to the SPU Write Outbound Interrupt Mailbox instead
  * of the SPU Write Outbound Mailbox, simply replace SPU_WrOutMbox
  * with SPU_WrOutIntrMbox in the following example.
  */
unsigned int mb_value;
do {
  /*
  * Do other useful work while waiting.
  */
} while (!spu_readchcnt(SPU_WrOutMbox));  // 0 \rightarrow full, so something useful
  spu_writech(SPU_WrOutMbox, mb_value);
```
How to Poll for or Block on an SPU Write Outbound Mailbox Available Event

```c
#define MBOX_AVAILABLE_EVENT 0x00000080
unsigned int event_status;
unsigned int mb_value;
spu_writech(SPU_WrEventMask, MBOX_AVAILABLE_EVENT);
do {
  /*
   * Do other useful work while waiting.
   */
} while (!spu_readchcnt(SPU_RdEventStat));
spu_writech(SPU_WrEventAck, MBOX_AVAILABLE_EVENT); /* acknowledge event */
spu_writech(SPU_WrOutMbox, mb_value); /* send mailbox message */
```

- **NOTES:** To block, instead of poll, simply delete the do-loop above.
PPU reads SPU Outbound Mailboxes

- PPU must check Mailbox Status Register first
  - check that unread data is available in the SPU Outbound Mailbox or SPU Outbound Interrupt Mailbox
  - otherwise, stale or undefined data may be returned

- To determine that unread data is available
  - PPE reads the Mailbox Status register
  - extracts the count value from the SPU_Out_Mbox_Count field

- count is
  - non-zero → at least one unread value is present
  - zero → PPE should not read but poll the Mailbox Status register
Example: PPE reads from the SPU Outbound Mailbox

```c
void *ps = spe_get_ps(speid); // system call assumed to return base address of problem state are
   // might vary, depending on libspe version

unsigned int mb_status;
unsigned int new;
unsigned int mb_value;
do {
    mb_status = *((volatile unsigned int *)(ps + SPU_Mbox_Stat));
    new = mb_status & 0x000000FF;
} while ( new == 0 );/*
* Issue an eieio instruction to ensure that the last
* Mailbox Status Register read is performed prior to the first
* SPU Write Outbound Mailbox Register read.
*/
__asm__("eieio");
mb_value = *((volatile unsigned int *)(ps + SPU_Out_Mbox));
```

Offsets into problem
state area
SPU Inbound Mailbox
SPU Inbound Mailbox

- The MFC provides one mailbox for a PPE to send information to an SPU
  - the SPU Read Inbound Mailbox.
- This mailbox has four entries
  - i.e. PPE can have up to four 32-bit messages pending at a time in the SPU Read Inbound Mailbox
SPU Read Inbound Mailbox Channel

- Mailbox is FIFO queue
  - If the SPU Read Inbound Mailbox channel (SPU_RdInMbox) has a message, the value read from the mailbox is the oldest message written to the mailbox.

- Mailbox Status (empty: channel count =0)
  - If the inbound mailbox is empty, the SPU_RdInMbox channel count will read as ‘0’.

- SPU stalls on reading empty mailbox
  - If SPE software reads from SPU_RdInMbox when the channel count is ‘0’, the SPU will stall on the read. The SPU remains stalled until the PPE or other device writes a message to the mailbox by writing to the MMIO address of the mailbox.

- When the mailbox is written through the MMIO address, the channel count is incremented by ‘1’.

- When the mailbox is read by the SPU, the channel count is decremented by '1'.
SPU Read Inbound Mailbox vs. SPU Write Outbound Mailboxes

- The SPU Read Inbound Mailbox can be overrun by a PPE.
- A PPE writing to the SPU Read Inbound Mailbox will not stall when this mailbox is full.
- When a PPE overruns the SPU Read Inbound Mailbox, mailbox message data will be lost.
How to write four 32-bit Messages to the PPU Read Inbound Mailbox of a Particular SPU from the PPE

void *ps = spe_get_ps(speid); // see previous example !
unsigned int j,k = 0;
unsigned int mb_status;
unsigned int slots;
unsigned int mb_value[4] = {0x1, 0x2, 0x3, 0x4};
do {
    /* Poll the Mailbox Status Register until the
    * SPU_In_Mbox_Count field indicates there is at
    * least one slot available in the SPU Read Inbound
    * Mailbox.
    */
do {
    mb_status = *((volatile unsigned int *)(ps + SPU_Mbox_Stat));
    slots = (mb_status & 0x0000FF00) >> 8;
} while ( slots == 0 ); // as long as full

} while ( k < 4 );
How SPU Reads From the Incoming Mailbox

```c
unsigned int mb_value;
do {
   /*
      * Do other useful work while waiting.
     */
} while (!spu_readchcnt(SPU_RdInMbox));
mb_value = spu_readch(SPU_RdInMbox);
```
Access to Mailboxes using macros defined in libspe.h (PPU) and spu_mfcio.h (SPU)
Mailbox Architecture

Find problem state address and offsets to memory mapped registers
Write directly into memory

Channel Instructions
spu_writech(<channel>, <value>)
spu_readch(<channel>)
spu_readchcnt(<channel>)

Macros defined in cbe_mfcio.h
(requiring system calls)
→ easier, but slower
Mailboxes Overview

**PPU (libspe.h)**

- `spe_stat_out_mbox(speid)`
- `spe_read_out_mbox(speid)`

*dataflow*

- `spe_stat_out_intr_mbox(speid)`
- `spe_get_event`

*dataflow*

- `spe_stat_in_mbox(speid)`
- `spe_write_in_mbox(speid)`

**SPU (spu_mfcio.h)**

- `spu_stat_out_mbox`
- `spu_write_out_mbox`

**MFC**

- `PPE mbox out_mbox`
- `PPE intr mbox out_intr_mbox`
- `SPE mbox in_mbox`

- `spu_stat_out_intr_mbox`
- `spu_write_out_intr_mbox`

- `spu_stat_in_mbox`
- `spu_read_in_mbox`

**PPU (libspe.h)**

- `spe_stat_out_mbox(speid)`
- `spe_read_out_mbox(speid)`

*dataflow*

- `spe_stat_out_intr_mbox(speid)`
- `spe_get_event`

*dataflow*

- `spe_stat_in_mbox(speid)`
- `spe_write_in_mbox(speid)`

**SPU (spu_mfcio.h)**

- `spu_stat_out_mbox`
- `spu_write_out_mbox`

**MFC**

- `PPE mbox out_mbox`
- `PPE intr mbox out_intr_mbox`
- `SPE mbox in_mbox`

- `spu_stat_out_intr_mbox`
- `spu_write_out_intr_mbox`

- `spu_stat_in_mbox`
- `spu_read_in_mbox`
PPE Access to Mailboxes

- PPE can derive “addresses” of mailboxes from spe thread id
- First, create SPU thread, e.g.:
  ```c
  speid_t spe_id;
  spe_id = spe_create_thread(0,spu_load_image,NULL,NULL,-1,0);
  ```
  - spe_id has type speid_t (normally an int)
- PPE mailbox calls use spe_id to identify desired SPE’s mailbox
- Functions are in libspe.a
PPE Mailbox Queue – PPE Calls (libspe.h)

- **“SPU outbound” mailbox**

- **Check mailbox status:**
  
  ```c
  unsigned int count;
  count = spe_stat_out_mbox(spe_id);
  ```
  
  - `count = 0` ➔ no data in the mailbox
  - otherwise, `count = number of incoming 32-bit words in the mailbox`

- **Get mailbox data:**

  ```c
  unsigned int data;
  data = spe_read_out_inbox(spe_id);
  ```
  
  - data contains next 32-bit word from mailbox
  - routine is non-blocking
  - routine returns MFC_ERROR (0xFFFFFFFF) if no data in mailbox
PPE Mailbox Queues – SPU Calls (spu_mfcio.h)

- “SPU outbound” mailbox
- Check mailbox status:
  
  unsigned int count;
  count = spu_stat_out_mbox();
  - count = 0 ➔ mailbox is full
  - otherwise, count = number of available 32-bit entries in the mailbox
- Put mailbox data:
  
  unsigned int data;
  spu_write_out_mbox(data);
  - data written to mailbox
  - routine blocks if mailbox contains unread data
PPE Interrupting Mailbox Queue – PPE Calls

- “SPU outbound” interrupting mailbox
  - Check mailbox status:
    - `unsigned int count;`
    - `count = spe_stat_out_intr_mbox(spe_id);`
      - `count = 0` ⇒ no data in the mailbox
      - otherwise, `count` = number of incoming 32-bit words in the mailbox
  - Get mailbox data:
    - interrupting mailbox is a privileged register
    - user PPE applications read mailbox data via `spe_get_event`
PPE Interrupting Mailbox Queues – SPU Calls

- “SPU outbound” interrupting mailbox
- Put mailbox data:
  
  ```c
  unsigned int data;
  spe_write_out_intr_mbox(data);
  ```
  - data written to interrupting mailbox
  - routine blocks if mailbox contains unread data
- defined in `spu_mfcio.h`
SPU Mailbox Queue – PPE Calls (libspe.h)

- **“SPU inbound” mailbox**
  - Check mailbox status:
    - unsigned int count;
    - `count = spe_stat_in_mbox(spe_id);`
      - `count = 0` ➔ mailbox is full
      - otherwise, `count` = number of available 32-bit entries in the mailbox
  - **Put mailbox data:**
    - unsigned int data, result;
    - `result = spe_write_in_mbox(spe_id, data);`
      - data written to next 32-bit word in mailbox
      - mailbox can overflow
      - routine returns 0xFFFFFFFF on failure
“SPU inbound” mailbox

Check mailbox status:

```c
unsigned int count;
count = spu_stat_in_mbox();
```

- `count = 0` ➔ no data in the mailbox
- otherwise, `count` = number of incoming 32-bit words in the mailbox

Get mailbox data:

```c
unsigned int data;
data = spu_read_in_mbox();
```

- data contains next 32-bit word from mailbox
- routine blocks if no data in mailbox
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