Fault Resilient Real-Time Design for NoC Architectures

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***Abstract*—Performance and time to market requirements cause many real-time designers to consider components, off the shelf (COTS) for real-time cyber-physical systems. Massive multi-core embedded processors with network-on-chip (NoC) designs to facilitate core-to-core communication are becoming common in COTS. These architectures benefit real-time scheduling, but they also pose predictability challenges. In this work, we develop a framework for Fault Observant and Correcting Real-Time Embedded design (Forte) that utilizes massive multi-core NoC designs to reduce overhead by up to an order of magnitude and to lower jitter in systems via utilizing message passing instead of shared memory as the means for intra-processor communication. Message passing, which is shown to improve the overall scalability of the system, is utilized as the basis for replication and task rejuvenation. This improves fault resilience by orders of magnitude. To our knowledge, this work is the first to systematically map real-time tasks onto *massive* multi-core processors with support for fault tolerance that considers NoC effects on scalability on an *real hardware platform* and not just in simulation.**

I. Introduction

ASIC-based cyber-physical systems are costly to design in terms of time and money. Multi-core COTS processors are becoming increasingly used in the high-end handheld market and are also seeing increased use in the lower-end embedded control market. An example is the Freescale 8-core PowerPC P4080 that is being marketed in the power utility domain for control devices. In such processors, traditional software design techniques coupled with increasingly smaller transistor sizes can negatively affect the real-time predictability and the fault reliability. Predictability challenges in multi-cores are due to non-uniform memory latencies [1] as contention on buses and mesh interconnects increases.

Another trend is an increase in transient faults due to decreasing fabrication sizes. These faults surface as single event upsets (SEU) that can render computation incorrect. SEUs are faults that can modify logic or data in systems leading to incorrect computational results or software system corruption, which can result in temporary or even permanent incorrect actuator outputs in control systems if not countered. SEUs have three common causes: (1) Cosmic radiation, particularly during solar flares, (2) electric interference in harsh industrial environments (including high temperatures, such as in automotive control systems) and (3) ever smaller fabrication sizes and threshold voltages leading to increased probabilities of bit flips (for all) or cross-talk (for the latter) within CMOS circuitry [2], [3].

For example, the automotive industry has used temperature-hardened processors for control tasks around the engine block while space missions use radiation-hardened processors to avoid damage from solar radiation. An alternative approach is taken by commercial aviation. The latest planes [4] (Airbus 380 and Boeing 787) deploy off-the-shelf off-the-shelve embedded processors without hardware protection against soft errors, such as the PowerPC 750. Even though these planes are specifically designed to fly over the North Pole where radiation from space is more intense due to a thinner atmosphere, processors deployed on these aircraft lack error detecting/-correcting capabilities. Hence, system developers have been asked to consider the effect of single-event upsets (SEUs), *i.e.*, infrequent single bit-flips, in their software design. In practice, future systems may have to sustain transient faults due to any of the above causes. COTS architectures are not specifically designed for real-time fault tolerance and contain few hardware-based fault mitigating mechanisms, such as processor radiation hardening. Previously, researchers have designed techniques to mitigate SEUs in software using task scheduling [5], [6], [7]. This often leads to sophisticated scheduling techniques utilizing alternate algorithms, re-execution, or replication. In contrast, we argue that massive multi-cores with NoC interconnects greatly simplify scheduling and allow high levels of replication.

In a system with replication of entire task sets under the traditional shared-memory model, considerable strain is placed on memory controllers due to compounded memory pressure and coherence traffic resulting in contention. This contention limits scalability and reduces predictability of advanced multi-core architectures. In spite of the potential drawbacks, multi-core COTS processors remain quite attractive for real-time systems. For example, ARM promotes “dark silicon” each real-time task is mapped to a separate core as cores are plentiful [8]. Scheduling then amounts to simple core activation thereby eliminating context switching costs and preemption delays. Such an abstraction also facilitates parallel, replicated execution and voting in n-modular redundant environments to increase reliability.

Contributions: This work introduces a Fault Observant and Correcting Real-Time Embedded (Forte) design for large multi-core architectures with NoC interconnects. The detailed contributions of Forte are as follows: (1) Forte provides a task abstraction framework that takes advantage of *message passing* capabilities implicit in NoC systems to *eliminate the use of shared memory*. Forte thus *increases the overall predictability* of the system as contention on the memory controllers is reduced. Furthermore, Forte improves *scalability* for contemporary mesh-based NoC architectures. (2) Forte *improves reliability* by provisioning simultaneous task models of varying complexity and measuring the strength of association (coherency) to *facilitate voting* in a modular redundancy scheme. (3) Forte further ensures sustained reliability by enabling fine-grained task rejuvenation. This includes the ability to replace faulted data models and to refresh rejuvenated tasks to align redundant models. Such rejuvenation is critical particularly for long-running or 24/7 control systems. Experimental results of Forte with a cyber-physical flight control software show improvements up to an order of magnitude in overhead reduction over standard shared memory implementations, reduced jitter and scalabil-

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ity. Reliability is improved in line with results reported for modular redundancy. Yet, Forte sustains these reliability levels through rejuvenation, which significantly increases reliability as opposed to a scheme without rejuvenation, as shown in experiments. Forte is a technique for improving the safety of systems by providing software redundancy for detecting soft-errors. Forte is limited in that it cannot protect from permanent hardware faults or failures. Thus, hardware redundancy is still a necessary addition to Forte for safety critical systems.

The remainder of this paper is structured as follows. Section 2 presents the design of our proposed framework. A case study developing an unmanned air vehicle control system is detailed in Sections 3 and 4. Section 5 provides the experimental framework. Section 6 presents experimental results. Related work is discussed in Section 7. The paper is summarized in Section 8.

II. Forte Design

This section provides an overview of the Forte framework to exploit massive multi-core processors to facilitate highly redundant cyber-physical systems. Careful use of this technique can improve system integrity in the form of protection from soft errors by providing a framework for running multiple concurrent versions of a task, called **shadow tasks**, and verifying their output coherence. The framework assumes that each task is permanently assigned to a unique set of cores and that the number of tasks in the system is less than the number of cores. The scheduling system is periodic with dynamic priorities based on relative deadlines. (Notice that scheduling amounts to activation/deactivation of tasks as only one task may be assigned to a core in our abstraction. Hence, we honor the periodicity of real-time tasks, yet scheduling becomes trivial as preemption never needs to occur.) Figure 1 depicts our model of a massive multi-core NoC processor. Our sample processor model contains 64 processing elements connected in a mesh grid. Each processing element contains a switch so that network communication and routing can be handled without additional overhead to the processing pipeline. NoC processors often support both static and dynamic message routing. Due to this, our framework operates agnostic of the underlying message passing API.

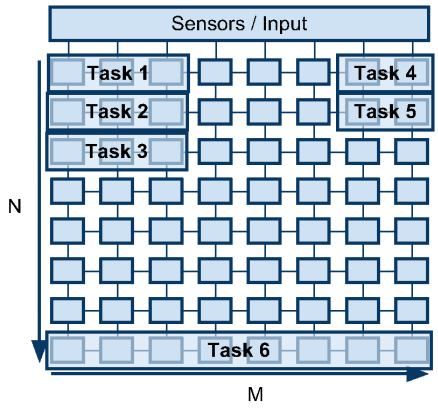

Fig. 1. Forte Task Layout Over Cores

Forte capitalizes on the additional processing elements available in advanced COTS processors to run multiple simultaneous system models. These models can vary in feature set and complexity, extending the model from the basic requirement, to a model with more precision/features to increase the system efficiency. We use the standard notation of $\phi, p, e,$ and d to denote phase, period, execution time, and deadline of a real-time task [9]. Using terminology from [10], we group the functional models and order them via complexity ranging from the most complex features to the "simple" baseline model. For example 1, consider two tasks $c =< \phi_c, p_c, e_c, d_c >$ and $s =< \phi_s, p_s, e_s, d_s >$, where c and s perform the same system function but c is a complex version of s, the baseline version. In Forte, we assert that $p_s = p_c$, since they provide the same system function, though e_c may be larger than e_s. We further assert that s and c generate output data where a coherency range can be determined. For additional redundancy, we consider two more tasks, c_{shadow} and s_{shadow}. These tasks are added to the system as mirror images of c and s, operating on the same data to validate the correctness of each model's output data. To formalize the framework, we extend the classic task model such that:

$$\tau =< I, O, T, C, R > \quad (1)$$

- I is the set of inputs i for the m shadow tasks in T;
- O is the set of outputs o of τ that must be validated for coherence prior to allowing the output change on the system to take effect;
- T is the sequence of shadow tasks $< t_1, t_2, ... , t_m >$ where each element t_i in T is ordered by a descending complexity coefficient k_i such that $k_1 \geq k_2 \geq .. \geq k_m$;
- C is the set of coordinates $< x_1, y_1 >, < x_2, y_2 >$ that enable the system to bound τ to a specific core within the architecture;
- R is the set of data within a task that must be transferred to a rejuvenated task to ensure convergence. If natural convergence is used $R = \emptyset$.

The Forte framework characterizes each task within the system with a set of inputs and outputs. Figure 2 depicts a Forte task where the input phase splits the data so that three redundant tasks of f can operate on separate models of the input data in parallel. We use the term f to describe the defining function (job) of the real-time task. When a task finishes execution it then sends the outputs to a coherence check that determines the correct output for the system. These sets allow tasks to execute independently or to be chained together to facilitate data flow within the system. Figure 3 depicts how the various tasks communicate data without using shared memory. The model forms an abstract chain: Once a task generates output data, its output data becomes the input data for a subsequent task. This model can be implemented on NoC architectures through explicit message passing.

A. Shadow Tasks

Forte is designed to exploit the high-level of concurrency that NoC architectures provide. Cyber-physical systems deployed in harsh environments are subject to *Single Event Upsets (SEUs)*. These are compelling reasons to utilize the multi-core paradigm and generate several models of a single task called shadow tasks, which improves the level of data integrity of the system. In the previous example from this section, c,c_{shadow},s, and s_{shadow} are considered shadow tasks of a single system level task τ. In Forte, shadow tasks are represented in a complexity ordered list. To state this more formally, for each shadow task t_i in T, there is a complexity coefficient k_i, such that

$$< t_i, t_{i+1}, ..., t_m > \implies k_i \geq k_{i+1} \geq ... \geq k_m \quad (2)$$

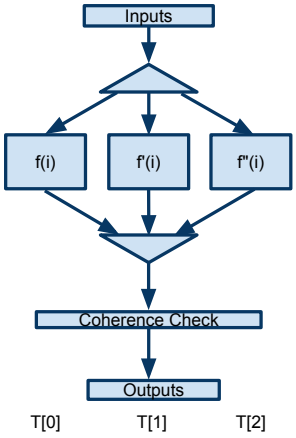

Fig. 2. Abstract Task Layout After Splitting

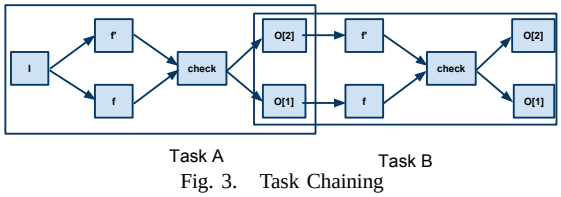

Fig. 3. Task Chaining

The complexity coefficient k_i is best generalized as a scoring value generated by deriving less precise real-time task models from the most sophisticated design. A degraded complexity model for real-time systems was put forth in [10]. In this work, a complex and a simple feature set for a given control task helped to increase the model safety. Deriving a score for k_i considers effects of a reduction in features and reductions in data precision or utilization for faster converging algorithms with a larger tolerance range ϵ.

B. Input

Real-time tasks have a variety of data models that can be supported in the Forte framework. Referring back to Figure 1, task 1 acquires input from sensors or other I/O devices that are not part of the task set. Task 2 derives input from task 1 and task 6 operates independently or receives input from a device that is pinned to the lower portion of the core layout. Supporting an abstract input set allows the framework to be flexibly used to deploy a variety of real-time tasks. Forte considers multiple data streams separated by complexity, shown in Figure 4. Streams enable shadow tasks of varied complexity to ensure that data is not unnecessarily losing precision by forcing a single stream of data.

In practice, input acquisition is a precondition for each task in Forte. If the input is derived from a sensor or other external hardware, it requires one of the shadow tasks to acquire the data and then distribute the data over the message passing network. If the input is derived from the output of another task, each of the shadow tasks must receive their input from a proceeding output of equivalent data complexity.

C. Output

Forte improves integrity by validating the coherency of each shadow task's data. A potential but undesirable result of this coherency validation is that the designer may have to reorder the code in control tasks to defer a decision until the shadow task decisions can be verified. Coherence formulations are determined by the system designer. Automatically identifying how to determine these is algorithm specific.

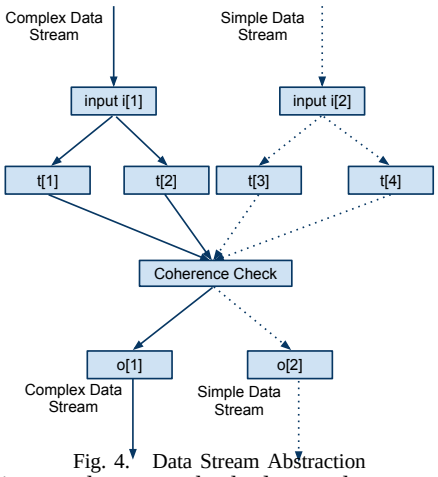

Fig. 4. Data Stream Abstraction

For a given task set, each shadow task operates on local data sets. Upon completing the necessary computation, the data is checked by the coherence-checking phase of the task. This may be performed by every shadow task or in a subset of them to reduce the data transfer cost. In the coherence check in Figure 4, shadow tasks $t[1]$ and $t[2]$ are of equal complexity and the data must match exactly. The same holds for $t[3]$ and $t[4]$. When this verification is complete, a range check is performed to validate that the data in the complex and simple streams are within a preset range. Certain features of the complex stream may not exist in a lower precision model. This makes it important to maintain multiple checks for each level of complexity. Successful coherency checks result in the mapping of output data to locations designated by complexity. This allows subsequent tasks dependent on this output to be mapped to the data of matching complexity. If the coherency checks fail, the failing task can be isolated to remove any impact it may have on the control system. If the failure is within the highest complexity model, subsequent shadow tasks that operate on that model can be canceled, allowing the system to rely on the less complex data models. If it is a lower complexity model that sustains the failure, data of the higher complexity models can often be filtered to allow a lower complexity model to continue operation. This output data flow is shown in Figure 4. The result of the complex data stream is filtered into the simple data stream in this case. When using fine grained coherence checks in a n-modular redundancy configuration rejuvenation can be used to repair the faulting task.

The formalization of input/output sets also supports feedback control loops. Forte allows data within the output set to be specified in the input set of subsequent tasks. This formalization supports task chaining. Feedback loops are supported as a chained loop of multiple tasks or the redirection of a single task's output back into its own input.

D. TDMA

Contention can hinder performance on message-passing networks, *e.g.*, when multiple fault models transmit their data to coherence checks in the Forte system. Tasks could potentially overwhelm routers or their buffers with adverse affects on performance. Forte addresses this problem by arbitrating the underlying NoC network through Time Division Multiple Access (TDMA). TDMA makes Forte more predictable by reducing contention on the message-passing network and facilitating the bounding of worst case behavior for all message-

passing phases. TDMA isolates core communication into global window frames. Any particular core is only able to transmit data during its predetermined frame. Using TDMA across all cores effectively allocates all links within the NoC to sender during their frame, guaranteeing that no two cores contend for a link during any period.

E. Task Rejuvenation

Real-time control systems are developed to run for extended periods of time, if not 24/7. They may thus be exposed to multiple failure events over the course of their lifetime. Single event upsets are handled through coherence voting and elimination of the faulty data. A subsequent second or third event upset to one of the remaining redundant tasks may leave the system without decision capability as to which the correct results is. The objective of rejuvenation is to correct the faulting model to ensure that resilience of the model is sustained. According to a study from the high performance domain [11], as devices advance and die sizes decrease, the projected failures per hour for a single node in an HPC system is $4.1x10^{-7}$. Another study [12] from the satellite domain using a hardened COTS multi-core device determines the failure rate to be $2.2x10^{-4}$ failures per hour. Both studies indicate that the probability of multiple-event upsets in a short time period is low. But if the runtime of the system is long, a second SEU is likely. This is the premise for rejuvenation ideas.

Forte addresses this challenge by supporting fine-grained rejuvenation as a part of the framework. Fine-grained coherence checks allow failing tasks to be identified. In Forte, an SEU is confined to a single task that is considered to have failed since tasks are associated with disjoint cores and do not share memory, i.e., only the failing task needs to be terminated. Subsequently, one of the remaining correct tasks supplies its output as input data to subsequent tasks of the terminated one during its rejuvenation. This is implemented as follows. The scheduler terminates the faulting task and creates a rejuvenated version of the task on the same core starting with newly initialized data values. The rejuvenated task is not caught up in its data output after such a restart and would fail the coherence check as thresholds would be exceeded. The coherence check is therefore temporarily relaxed to only validate the outputs of the remaining tasks (ignoring the rejuvenated one).

Coherence validation via voting is deferred until the rejuvenated task converges with the correct models in terms of its output. Many control algorithms exploit convergence algorithms in feedback loops to guarantee stability, i.e., they will naturally converge over a period of time if the output is dependent on the input. In other cases, running state is maintained between each job invocation of a task so that models do not converge by itself. Here, the state of one of the remaining (correct) tasks is utilized to allow the rejuvenated task to catch up. Forte supports data refreshing of rejuvenated tasks as follows. A correct task is designated by the coherence module to refresh a rejuvenated task with local memory values specified during system design. These memory regions are transferred to the rejuvenated task in between job invocations to assure consistency. Data refresh is a requirement for non-converging algorithms. But it can (and often should) also be utilized to more quickly catch up with the correct tasks for converging algorithms. This reduces the vulnerability window to receive another SEU while operating under degraded redundancy (e.g., dual redundancy) during rejuvenation. After data refreshing (or convergence without refresh), the coherence validation can reactivate voting again upon reception of outputs from the reborn task within thresholds.

III. UAV Application

The next two sections describe our experimental implementation of the Forte design using a cyber-physical control system. This section describes the control system and its tasks. The next section describes the changes necessary to move the control system into the Forte framework. To evaluate the design, we selected Paparazzi [13], a traditional shared memory real-time control system. Paparazzi is an unmanned air vehicle (UAV) control software. We ported it using the Forte design framework and evaluated it on a hardware NoC architecture. Our port of the Paparazzi control system is based on a java implementation [14] that we rewrote in C++. Paparazzi is structured as two separate sets of real-time tasks that enable a switch between manual control of the aircraft and autopilot mode. These modes are detailed as Fly-By-Wire (FBW) and Autopilot (AP). The basic structure of Paparazzi allows only the FBW mode to control the servos. However, when there is no pulse position modulation (PPM) control, the autopilot mode sets the actuation by controlling the values that the FBW mode uses to control the servos. This relationship is detailed in Figure 5.

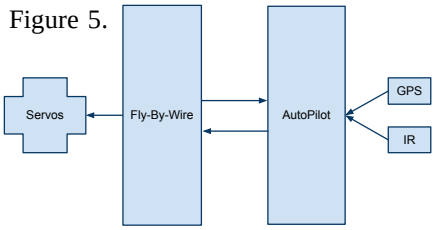

Fig. 5. Paparazzi Design

A. Paparazzi Autopilot-Base Design

The basic design of the shared memory version of Paparazzi uses several shared objects accessed various tasks to calculate vectors to control the UAV. This information consists of a navigator, estimator, and a flight plan. The following paragraphs will briefly cover each task and how it operates on these shared data structures in order to illustrate later how to redesign for a message-passing framework. The basic task layout for the auto pilot module with task dependencies and data flow are shown in Figure 6. **Navigation Task:** The navigation task is responsible for taking information from the GPS device, determining the current location of the UAV and then storing the values into the estimator data structure for later tasks that cannot read the GPS data. It then compares this information against the flight plan and determines target metrics for the UAV to meet the flight plan. **Altitude Control Task:** The altitude control task is responsible for determining the control values to reach/maintain the desired UAV altitude. It first ensures that the system mode is set to allow autopilot control. It then obtains data from the estimator's z coordinates and determines the error from the desired altitude. It then uses this error factor to determine any corrections and commits them to one of the shared memory objects. **Climb Control Task:** The climb control task is responsible for determining the system's output in terms of thrust and pitch in order to maintain the necessary altitude. It takes as input the altitude determined in

the altitude control task and the z directional speed vector determined in the navigation task. It uses these inputs to calculate the necessary pitch and thrust to control the altitude of the UAV's vertical changes. **Stabilization Control Task:** The stabilization control task uses data from the infrared (IR) device, the climb control task, and the navigation task. This task is responsible for determining the roll and any changes to the pitch. The stabilization control task in this implementation is also responsible for transferring the data to the FBW task that updates the actuation on the servos. The data sent is the pitch, roll, throttle, and gain to control the servos. **Radio Control Task:** This task takes the last radio control command from the FBW module and stores the data in the autopilot in case it needs to take over control.

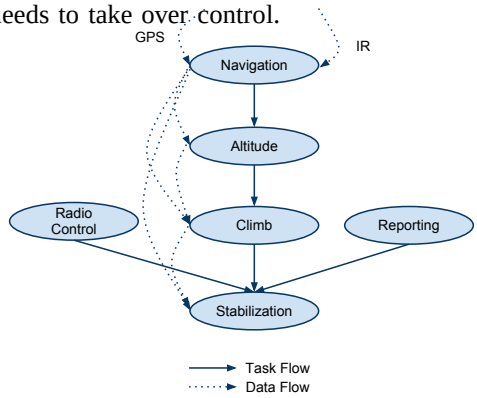

Fig. 6. Auto Pilot Task and Data Flow

B. Fly-By-Wire Base Design

The Fly-By-Wire (FBW) task set is used to control the servos and to take control from the ground control unit, the latter of which is not exercised in this implementation. The task layout of the FBW module is shown in Figure 7. **Pulse Position Modulation (PPM):** The PPM task receives the radio commands from the PPM device and uses them to control the servos of the UAV if the autopilot mode is not enabled. **Transfer to Autopilot:** This task takes the message retrieved from the PPM device and transfers it over the systems designated bus to the Radio Control Task. **Check Fail Safe Mode:** This task controls whether the auto pilot or the PPM device is controlling the UAV. It validates several device-based metrics to determine if the device is still receiving signals from the PPM device or if a fail-safe mode has been activated. **Check Auto Pilot:** This task controls the servos based on data received from the AP. The task receives data from the stabilization control task over the systems specified bus and then transfers these control values to the servos for actuation. **Flight Model and Simulated Devices:** In order to function appropriately Paparazzi requires a GPS device, IR device, and a functional flight model. The Flight model specifies flight dynamics based on the rudimentary version found in the Paparazzi open source code. The GPS device infers several metrics based on its current position, its last position and the change in time. The IR simulates a dual axis differential IR device, that uses IR temperature readings between space and the earth to stabilize the roll and pitch of the aircraft. The output data from the IR device is critical in the stabilization task.

IV. Forte Implementation

The Forte implementation follows the design in respecting the relation between input and output tasks, supporting the

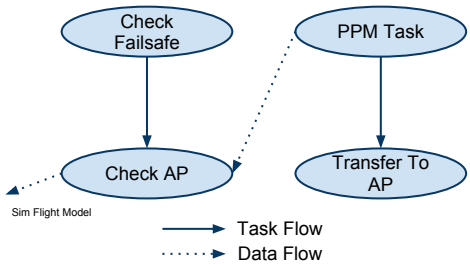

Fig. 7. Fly-By-Wire Task and Data Flow

fault model of n-modular redundancy with coherence checks on outputs and optional task rejuvenation.

A. Input and Output Tasks

Implementing Paparazzi using the Forte design required analyzing the shared memory accesses that occurred within the task set and expressing them as data-flow relationships between tasks. The original implementation of Paparazzi uses logical objects to store data in containers. This eased programming requirements in that it made the data logically organized. However, it also made all data in these objects globally accessible. While this is suitable for single-core implementations, using shared data in multi-core scenarios adds overhead. We remedied this by transforming data flow relationships to remove shared object containers altogether. They were replaced by data designated in two ways.

First, we utilize local data when data is only operated on within a task. The majority of data in our implementation could be categorized as local data. This contains all temporary variables and most of the state variables that update the primary flight metrics during operation.

Second, we utilize remote data. This data is stored locally but the actual data values originated else-where and are communicated between cores via sends and receives. Remote data values are written to local memory of the task before the task is released. In Figure 6, the dotted lines represent the flow of remote data in the auto pilot module.

We then converted each task into Forte tasks. Each Forte task consists of an input phase, a computation phase, and an output phase. The input phase of each task is generic. The task simply receives data and stores it in local memory for subsequent execution. Task computation differs from the shared memory version only in that instead of operating on global containers all data is local to the tasks core. The output phase sends any data to subsequent tasks according to the data flow specifications.

B. Scheduler

In the introduction of this paper, we made the claim that massive multi-core architectures could ease the problem of task scheduling. Trends in the market indicate that in the near future architectures with tens if not hundreds of cores will be arriving. In the past, processing resources were in heavy contention and sophisticated scheduling techniques were needed to arbitrate access to limited resources. The term limited can no longer be used to describe processing resources for massive multi-core architectures. For the Forte implementation of Paparazzi, the scheduler is a simple periodic scheduler. The scheduler statically deploys each task to its own core where it remains stationary. Taking advantage of the massive multi-core architecture, no tasks shared a core. Scheduling thus reduces to core activation/deactivation to release or terminate a task. Each task is then set to sleep until it receives a

NoC-based message from the scheduler core waking it up to perform its task. The impact of the sleep state is significant in terms of power consumption. As the number of cores on these architectures scales up, that ability to power them simultaneously will become a serious challenge. In order to limit the scope of the power consumption of such chips, many chip designers are implementing low power sleep modes with instant-on functionality. Other research has contributed gating on routers/switches during periods when they are not used [15]. This has shown to reduce power consumption for these processors. Such sleep states, optionally combined with gating, enables software to constantly turn off and on the resources needed while conserving power. A possible expansion to this work would be the exploration of distributed operating system (OS) functionality for such processors. One limitation in our current experiments is that we do not explore OS feature duplication. However, we feel these problems could be remedied as some architectures already support individual OS images per core. This added redundancy could be used to protect systems from SEUs affecting OS faults, which is beyond the scope of this work.

C. Fault Models

To simplify our experimental implementation, we integrated an n-modular redundancy configuration using the Forte model instead of a Simplex implementation. In our evaluation, we use a triple modular redundancy. This shows the flexibility of the architecture in that can use Forte's design for three completely simultaneous instances of Paparazzi. This enables coherence checks to identify the faulty model in times of failure so that voting can occur to determine which model controls the simulated servos.

D. Coherence Checks

We designed several coherence checks to enable robust fault checking for our Paparazzi implementation. Since our fault model in Forte was designed with redundancy tasks, our coherence checks simply verify data consistency. Each coherence check is designed as a sporadic task that immediately follows the execution of a system task in the Paparazzi suite using precedence constraints. Each coherence task is assigned to a specific system core. When the coherence task receives data from the first model, it sets a timeout in order to not wait indefinitely for the remaining models to transmit their data. When all of the models have transmitted the data, the coherence check validates the data. When there is a validation error, the coherence check uses a $2/3$ majority. It determines the failing model and notifies the voting routines to prevent the faulting model from controlling the system servos. When a timeout occurs coherence is checked between the models that did submit data, any models that did not submit data are considered to have failed.

E. Rejuvenation

Rejuvenation is implemented in Forte in two ways. The feedback control algorithms support natural convergence and, as such, just require a restart mechanism and a warm up phase to re-enable coherence validation. Paparazzi utilizes such natural convergence, i.e., our implementation exploits this restart capability. In addition, rejuvenation with refreshed data was realized as an optional extension. This allow us to compare the time (overhead) for convergence with and without refresh. To facilitate rejuvenation under data refresh, the coherence module uses the message passing network to indicate the source data refresh, i.e., one of the remaining correct tasks (cores). Refresh data is transmitted during the next idle phase to ensure non-interference with real-time deadlines of the correct tasks. The refresh data is also received during the idle phase of the restarted task as redundant tasks are harmonic (not only in period but also in idle phase). Received data subsequently refreshes uninitialized state in tasks, either to ensure that outputs are within coherence thresholds or, as in the Paparazzi example, to speed up convergence among the redundant tasks.

Forte rejuvenation has an impact on WCET bounding that is important to the real-time aspects of CPS systems. In defining rejuvenation, we impart two different techniques for data correction that vary with regard to how rapidly data can be corrected. The first technique is natural convergence. It requires a task refresh that is handled by re-instantiating the task. This will impact performance because re-initialization of tasks leads to a task warm-up phase. This effect will not lead to an increase in WCET bounds of the task itself since a cold start has to be considered for the initial startup in the bounds. Additional conditionals must be used during the coherence measurement tasks to temporarily ignore data from the faulted task. This only adds the overhead of a single conditional check to the WCET bound for the coherence task since less work (no coherence check) is performed if results match. The second model, a data-driven approach, is impacted by the same startup costs that affects natural convergence and adds the nominal cost of sending duplicate data from a healthy data model to a restarted data model. This additional data doubles the information transfer from a source and must be considered in bounding WCET.

F. TDMA

For the implementation of TDMA in Forte, we assume a target multicore architecture with a NoC interconnect, such as the Tilera Tilepro 64. We assume a globally accessible and synchronized cycle count register on each processor. We thus are able to implement self-reference based TDMA frame checking within the message passing logic of Forte. We leave the task of frame scheduling to the application designer. However, as the amount of cores continue to increase in NoC architectures, it may be important to consider partitioned or phase-based TDMA. This could reduce WCET bounds due to a decrease in total frames. In implementing our experiments with Forte, there were clear and non-intersecting task group phases in the Paparazzi that allowed us to eliminate unused frames during each phase to improve performance and decrease bounds. For the purpose of Forte, we only implemented TDMA for access to the explicit message passing networks. Memory accesses issued during the execution of a Forte task were not subject to TDMA.

V. Experimental Framework

Our experiments were conducted on a Tilera TilePro64 development board. This platform features a 64 tile (core) chip multiprocessor (CMP) suitable for the embedded space with lower power requirements [16]. The Tilera platform has been selected for satellite deployment. Tilera processors support both message-passing and coherent shared memory models, and the choice is up to the user. Tiles are connected by

multiple meshed NoCs that support memory, user, I/O, and coherence traffic on separate interconnects. Each tile processor is equipped with level 1 caches and split TLB making each core a fully independent processor. Our experiments were conducted on a Tilera Tilepro 64. Each core contains a 16KB L1 instruction cache, an 8KB L1 data cache, and an 64 KB L2 unified cache. For evaluating our framework, we implemented the PapaBench real-time task set from the Paparazzi UAV cyber-physical system. Two implementations were created for evaluating not only the framework's fault resilience but to also compare computational jitter in systems relying on shared memory vs. message-passing. The shared memory task sets follow the proposed model in the paper (but with input and output phases integrated with computation phases of tasks). Due to the integrated nature of memory accesses into the processor pipeline, we did not employ any TDM techniques in the shared memory portions of the experiments. Figure 8 depicts the system layout of the control tasks identified by their abbreviated name combined with their execution identifier *e.g.*, CC2 is Climb Control Task 2 (see Section III for task identifiers). The figure illustrates the linear task layout across the tiles. This layout is agnostic to the execution models (shared memory vs. message-passing). All experiments using more than two tasks arbitrate access to the NoC using TDMA as described in previous sections. This reduces the impact of NoC effects on the system.

	0	1	2	3	4	5	6	7
0	OS	Scheduler	FM Sim 1	FM GPS 1	FM IR 1	Nav 1	Alt 1	CC 1
1	Stab 1	Rad 1	Report 1	Fail Safe 1	Send To AP 1	Check AP 1	PPM 1	Co - Check
2	FM Sim 2	FM GPS 2	FM IR 2	Nav 2	Alt 2	CC 2	Stab 2	Rad 2
3	Report 2	Fail Safe 2	Send to AP 2	Check AP 2	PPM 2	FM Sim 3	FM GPS 3	FM IR 3
4	Nav 3	Alt 3	CC 3	Stab 3	Rad 3	Report 3	Fail Safe 3	Send to AP 3
5	Check AP 3	PPM 3						
6								
7								

Fig. 8. Paparazzi Task Layout

We conducted experiments with both the message-passing and shared-memory approaches using triple concurrent redundancy to evaluate the effectiveness of the Forte framework. We employed targeted fault injection in each of the models by generating data errors to evaluate the effectiveness of the coherency checks. Currently, Forte is unable to handle OS-based faults or hardware faults. For the former, we argued previously that OS duplication is a feature already supported by these architectures but not explored in the course of this work. For the latter, we maintain that any software-based redundancy would be useless without employing redundant hardware as a primary fail-safe technique. As such, this work is not a replacement for hardware redundancy but rather complements it to increase resilience to faults. We injected faults into both code segments and actively used data segments. Faults were dynamically inserted into the code and configured to be trigger randomly during the execution of the control system through the flight path. To model full redundancy, we duplicated the simulated UAV hardware so that each model operated on unique device inputs.

VI. Experimental Results

Table I depicts the number of injected faults that are detectable (resulting in output faults) and the number of actually recognized faults. The results indicate that all detectable faults were recognized and subsequently averted using voting in the coherence checks. We implemented a single coherence check to validate system data prior to servo actuation. The coherence check assessed the output data that was passed over the peripheral bus to the servo controller. We only included outcomes from SEUs that created an actual effect on the output state of the running systems. Faults were categorized as follows: (1) Downstream data errors: prior to servo actuation, outputs of the models were compared for consistency. By using three duplicated models, the faulting model is defeated (voted out). (2) Read-only (RO) memory upsets caused one of the models to fault. When this occurred, one model failed the coherence check through a timeout mechanism set by the coherence check's data deadline.

SEU Type	Detectable SEU Count	Recognized
Heap Flip	15	15
Device Failure	3	3
Stack Flip	10	10
Read Only Flip	4	4

TABLE I
Fault Injection Evaluation

The next experiment exemplifies one of the major benefits of the message passing design over shared memory. Figure 9 depicts the computational cost (in cycles) for accesses to data subject to coherency checks for both models. These results measure the coherence within the climb control model that maintains computational control over five of the system control variables. This coherency check validates the consistency of the three simultaneous climb control data sets. As Figure 9 indicates, shared memory results in an order of magnitude performance penalty compared to message-passing. The overhead of the latter is due to maintaining coherency for remote writes for the validation checks. The message-passing model eliminates the need for coherence and reduces conflicts on the interconnects resulting in more predictable and lower

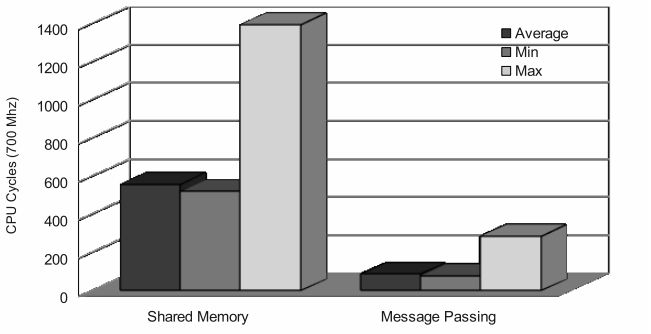

Fig. 9. Overhead of Coherence: Shared Memory vs. Message Passing

Figure 10 depicts the overheads for computing integer data in the climb control task. These results show stable timings for task computation with message passing, much in contrast to shared memory. We evaluated integer computations because of a lack of hardware floating point units (FPU) on the Tilepro64. This data demonstrates how easily contention on the NoC results in jitter. In this result, three simultaneous models are executing while the previous results utilized only one active tile during the actual check. Note that when multiple tiles

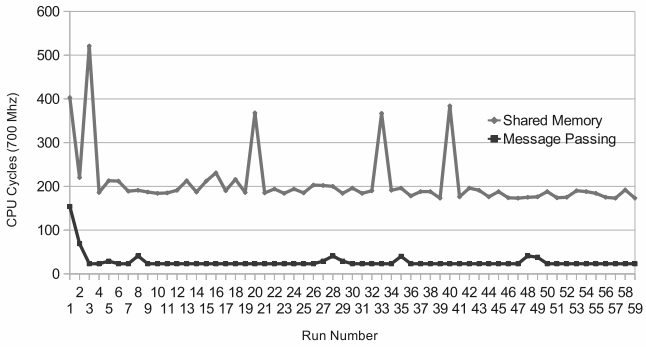

Fig. 10. Climb Control Task Jitter: Shared Memory vs. Message Passing

are active simultaneous jitter is easily introduced into shared memory accesses. In contrast, TDMA arbitrates NoC access for messages.

SEU Scheme	Time To Repair	Mean Time to Failure
No Rejuvenation	∞	157 Days
Natural Convergence	8 (2s)	$2.27x10^8$ Days
Data Driven	1 (250ms)	$2.05x10^9$ Days

TABLE II
REJUVENATION: TIME TO FULL RESTART

We implemented a naturally converging model and a data refresh model to assess the benefits of rejuvenation when SEUs affect task data. To compare the models, it is necessary to measure the time from failure until triple redundancy is restored, i.e., voting within the system can restart. Table II depicts this as the time to repair for each scheme. These results do not take into account hardware failures or SEUs affecting the OS. Instead, these results only consider software task sets. Column two indicates that natural convergence took eight job cycles (periods) before voting could restart while rejuvenation with data refresh was able to accurately measure coherence one job (period) after the original failure. Column three assesses the mean time to failure (MTTF) for each scheme. Without rejuvenation, the model to derive data for the second row follows the standard MTTF calculation $MTTF_{TMR} = 5/(6\lambda)$. The model with repair via rejuvenation used to derive results for the third and fourth rows is based on a modified Markov formulation that calculates MTTF as $MTTF_{TMR-Repair} = 5/(6\lambda) + \mu/(6\lambda^2)$ [17]. μ is the maximum number of repairs that can be performed within an hour. We evaluated our model based on an SEU rate of $\lambda = 2.2083x10^{-4}$ derived from a radiation-hardened Tilera processor for these results [12]. This provides a worst-case λ as the processor is hardened and the error rates are evaluated in space making λ higher than values derived for single-node failures for terrestrial applications, e.g., λ values reported for HPC environments. As can be seen from the results, rejuvenation increases reliable operation by six to seven orders of magnitude.

The experiments thus far assess the cost of communication in a cyber-physical system that only exercises some aspects of Forte's design. To evaluate the limits of Forte, we implemented a micro-benchmark that transfers a 0.5KB payload of data between a pair of processors and then proceeded to increase the number of transferring pairs. The benchmark utilizes both shared memory and message passing to evaluate the cost of data transfers. Hashing is a technique where memory addresses are uniformly distributed across the L3 cache by the hardware. Notice that this is a virtual L3 cache implemented through a hypervisor by distributing memory references over the L2 caches of all cores. The distribution uses a home-based protocol where the hash of a shared memory address redirects a look-up to a home core over a specific coherence interconnect on the NoC. Hashing can thus increase the performance of shared memory by reducing the average distance to cached data and by increasing cache capacity of L3 to the aggregate of all L2 caches. This effect is demonstrated in Figure 11. Hashed shared memory outperforms the non-hashed counterpart on average. However, even with a significant reduction in the cost of shared memory accesses, message passing outperforms shared memory in both configurations. Furthermore, we capture the best-case and worst-case transfer latencies illustrated by the top/bottom of the error bars in Figure 11. The results show a significant disparity that becomes apparent in both of the shared memory experiments as the number of transferring processors are scaled up. With an increasing processors count, the worst and average case transfers rise significantly due to NoC and cache contention. Under message passing, in contrast, virtually no changes in the best, worse, and average cases are experienced.

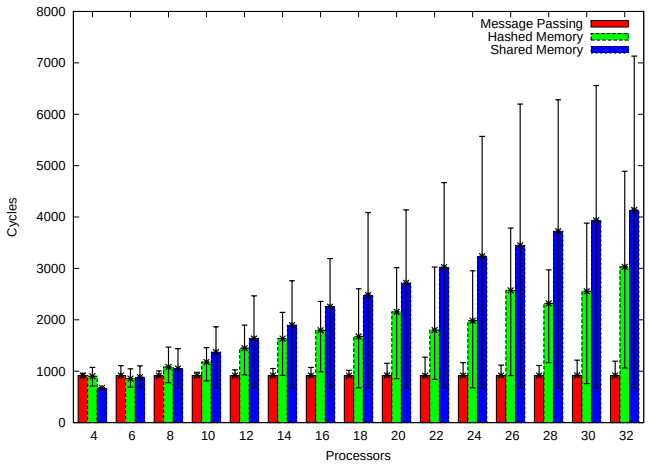

Fig. 11. Transfer Overhead: Shared Memory vs. Message Passing

Next, we evaluated the scalability of the Forte design. We ran a single Paparazzi model of the full system in this experiment. The number of replicas of the altitude control task was scaled up gradually from 10 over 20 to 30 redundant instances. All replicas were executed in parallel on separate cores. This raised the overall utilization to 45 cores for the Paparazzi task set including the scheduler and coherence check. Figure 12 depicts the cost of data transfer/computation (in cycles) over multiple benchmark run for 10, 20 and 30 replica. A relatively inconsistent access cost is incurred with 30 replica cores for shared memory. Interestingly, a consistent additional overhead of approximately 50 cycles is observed for shared memory using 20 and 30 replica cores relative to just 10 cores, which can be accounted to scalability limits of the coherence protocol due to contention on the coherence interconnect. In contrast, additional replicas have virtually no measurable effect on the overheads for message passing (without L3/hashing) as TDMA arbitrates NoC access when messages are transferred. The occasional spikes in these results are caused by the virtualization layer in our experimental platform, which periodically activates a required monitoring daemon resulting in system noise. Such daemons would need to be eliminated or modeled as a separate task to meet real-time requirements.

Overall, the results indicate superior performance, increased predictability and reduced jitter of pure message passing (without any background coherence protocol) in this massive multi-core platform with a mesh-based NoC. Performance and predictability benefits of message passing over shared memory improve as the number of utilized cores increases, *i.e,* message passing scales in contrast to shared memory programming. The cause of these benefits lie in the potential of one-sided communication and TDMA arbitration of message passing in a push-based (explicit) access model. These advantages cannot be matched shared memory protocols with its pull-based (implicit) on-demand access requests and its required hand-shake semantics of the coherence protocol.

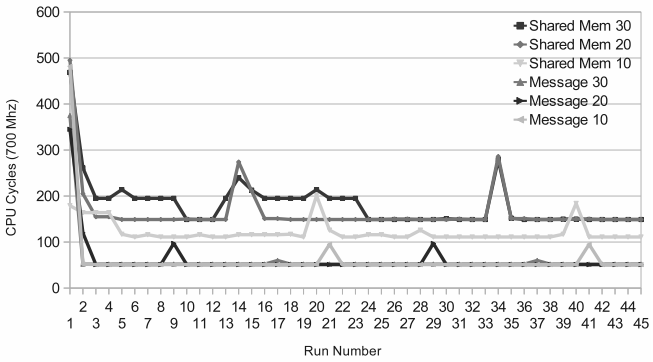

Fig. 12. Scaling Contention: Shared Memory vs. Message Passing

VII. Related Work

Our study appears to be the first one combining a *real* implementation on a *massive* multicore with 64 cores with real-time constraints and fault tolerance. Prior work was strictly simulation based, let it be for studying topologies for *simulated* shared memory architectures [1], [18] or fault tolerance with hardware support in a simulated NoC environment [19]. One notable exception is the Multikernel (aka. Barrelfish) system that indicated that message passing can be superior to shared memory in an SMPs system using Hypertransport [20]. In contrast, our work is not on SMPs and focuses on much larger core counts that introduce scalability problems due to NoC resource contention on a single processor die. Another exception is Tilera's iMesh paper [18], which investigates higher-level software overheads of the iLib abstraction for buffered channel and high-level dynamic messaging vs. row channels. Our work provides more insight on jitter and clarifies the overhead of shared memory accesses vs. the benefits of a much lower level messaging layer, which exposes the true overheads at the lowest software layers.

There is significant related work in the area of fault tolerance. Past approaches utilize scheduling, replication, or radiation hardening to achieve fault tolerance. Scheduling techniques, such as in [5], [6], [7], often introduce sophisticated scheduling policies to track faults. In particular, [5] introduces a last chance scheduling technique with the notion of task alternates to correct data in times of faults. A complicated scheduling algorithm then delays the execution of these alternates until the last possible moment to provide a fault tolerant schedule. We use advanced multi-core architectures to remove the need for such sophisticated scheduling by enabling the software to run alternates simultaneously at virtually no additional resource cost.

There exists a significant amount of work on detection of and protection against transient faults. Hardware can protect and even correct transient faults at the cost of redundant circuits [21], [22], [23], [24] Software approaches can also protect/correct these faults, *e.g.*, by instruction duplication or algorithmic design [25], [26], [27], [28], [29] Recent work focuses on a hybrid solution of both hardware and software support to counter transient faults [30], [31], [32]. Such hybrid solutions aim at a reduced cost of protection, *i.e.*, cost in terms of extra die size, performance penalty and increased code size. Hybrid approaches have been proposed for selectively protecting hardware regions, for control-flow checking and for reduced instruction and data duplication in software [30]. Data representations, however, have been widely ignored. Radiation hardening is another common technique in fault protection for real-time systems [33], [34] with overheads in costs and speed. In contrast to our work, these solutions either promote hardware approaches or do not consider massive multi-cores (or even real-time systems).

Modular redundancy is a replication technique[35]. This work provides an easy to implement and validate approach to ensuring fault tolerance. The technique has been used widely in research. [19] describes a heterogeneous NoC architecture to implement triple modular redundancy. This work focuses on a specialized architecture that supports multiple levels of hardware integrated fault detection. This work uses TDMA on a NoC to interconnect the various IP elements in the architecture. Our work also utilizes a replicated task mapping but differs in that it is a pure software approach that enables comparisons of varying task complexity models with COTS applicability. More significantly, their study is based on hardware simulation, ours is an actual implementation on a hardware platform. Theirs covers a small number of cores, ours is for *massive* multicores with high core count, which creates novel challenges for harnessing NoC contention.

Rejuvenation [36], [37] is a technique originally introduced as a software restart technique to protect long-running software. Rejuvenation is often associated with rebooting. A major hurdle in software rejuvenation is data loss due to the rejuvenation. Forte uses software rejuvenation to maintain reliability in the control system. Data loss is circumvented through selective rejuvenation and data refreshing from validated data models.

VIII. Conclusion

We have presented the design of Forte, a framework that utilizes massive multi-core NoC architectures in order to create a reduced jitter and fault tolerant cyber-physical environment. The primary tenets of this approach encompassed systematic restructuring of traditional real-time tasks to eliminate the use of shared memory by instead relying on message passing to move data between tasks. By reducing contention on memory controllers, it becomes more feasible to scale up the number of cores while sustaining performance and predictability. This enables support for fault tolerance through replicated real-time tasks combined with consistency verification and task rejuvenation using modular redundancy. Our results feature experiments with triple modular on-chip redundancy for a UAV control system and illustrate capabilities of Forte to detect errors and correct tainted results due to data errors, such as SEUs. We also show that by putting greater emphasis on message passing and eliminating shared memory accesses, we are able to increase predictability and decrease overheads by

up to an order of magnitude. System reliability can be further increased by six to seven orders of magnitude when triple modular redundancy is combined with naturally converging and refresh-assisted rejuvenation, respectively.

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